44. The semiconductor structure of claim 39, further comprising:

a metal layer disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the metal layer.

45. The semiconductor structure of claim 39, further comprising:

a metal layer disposed on the substrate;

a second dielectric disposed on the metal layer; and

wherein the first layer of spin-on glass is disposed on the second dielectric.

46. The semiconductor structure of claim 39 wherein the first dielectric comprises a low-temperature oxide.

47. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass and a planarized portion of the first dielectric.

48. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass, a planarized portion of the first dielectric, and a planarized portion of the first layer of spin-on glass.

REMARKS

Claims 1 – 48 are pending in this broadening reissue application.

The Applicants have added new claims 23 - 48 to broaden the scope of protection to their invention.

The Applicants have added no new matter to the reissue application.

In light of the foregoing, original claims 1 – 22 and new claims 23 – 48 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a telephone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully submitted,

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